

Nanocrystalline Silicon Layers for the Application in Silicon Heterojunction Solar Cells

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Abstract. After application in thin-film silicon tandem solar cells and in lab-scale silicon heterojunction (SHJ) devices, doped nanocrystalline silicon (nc) layers now arrived on the industrial stage. Despite their challenging deposition, the benefits they hold with respect to even higher device performance compared to their amorphous counterparts are significant and justify additional effort. In this contribution we report on developments towards industrially applicable processes for n- and p-doped silicon layers, nc-Si(n) and nc-Si(p), and their implementation in SHJ cells. Our investigation focuses on the impact of deposition temperature (T_{dep}) and the need for a thin oxide layer to promote fast nucleation of thin, sufficiently crystalline, doped nc-Si films in a single deposition chamber powered at 13.56 MHz. We identified main challenges for thin film and contact engineering and reached efficiencies of 23.0% with n- and 23.1% with p-type nc-Si approaching cell performances of our process of record based on amorphous Si (a-Si) layers.

Keywords: Silicon Heterojunction Solar Cells, Nanocrystalline Silicon Layers, 13.56 MHz Deposition Frequency

1. Introduction

In contrast to a-Si, nc-Si holds the potential to reduce parasitic absorption and improve contact resistivity [1]. This is due to its indirect band gap and higher doping efficiency, respectively. Optimizing cell performance, the following requirements must be met: (1) fast nucleation of nc-Si layers on the intrinsic a-Si(i) passivation layer, avoiding a thick, insufficiently doped a-Si incubation layer; (2) pristine passivation layers; (3) high crystallinity to benefit from the superior material properties [2]. Finally, (4) the deposition should follow a lean, low-cost process flow that requires only minor adaptations to the PECVD tool and process sequence.

Strategies to achieve this have been developed leading to excellent cell performance on both sides contacted [3, 4] and interdigitated back-contacted SHJ devices [5, 6]. Here we report on developments of nc-Si layers, the impact of deposition temperature (T_{dep}) and the necessity for an ultra-thin oxide layer (SiO_x) at the interface between a-Si(i) and the doped nc-Si layer for application of nc-Si in full-area M2 SHJ devices. In the SHJ devices either the a-Si(n) or a-Si(p) layer was replaced by a nc-Si layer. The SiO_x Further we are aiming to remain within current industrial standards concerning the deposition technology for the a-Si-layer stack of SHJ devices (PECVD at 13.56 MHz, standard precursor gases).

Regarding the SiO_x interlayer, a vacuum break after a-Si(i) deposition is currently part of the industrial deposition sequence. The exact process details depend on the strategy for wafer flipping and cross contamination management. Instead of a VB also a separate PECVD-based SiO_x layer after a-Si(i) before nc-Si(doped), can be implemented in the process sequence which enables a controlled process conditions for the SiO_x layer growth as we show in this work. Finally micro doping of the SiO_x layer is investigated with the aim to improve the contact properties.

2. Experimental

The processes we developed are based on standard precursor gases silane, hydrogen (H₂), carbon dioxide (CO₂), phosphine (PH₃ 5% in H₂) and trimethylborane (TMB 2% in H₂). The layers were deposited in a parallel plate PECVD reactor at 13.56 MHz, in a high-power, high-pressure regime at 140 and 180°C. Before the deposition of the nc-Si layers a vacuum break (VB) or CO₂ plasma treatment was applied to grow a SiO_x interlayer which accelerates the nc-Si nucleation on the a-Si(i) passivation layer. The layers were characterized both by spectroscopic ellipsometry and film resistivity measurements as well using contact resistance measurements using test structures.

In a second step we fabricated M2-sized SHJ rear emitter cells, using n-type Cz wafers and applying either a-Si(i)+n-type layers (a-Si or nc a-Si(n)) at the front and a-Si(i) + a-Si(p) at the rear or a-Si(i)+p-type layers (a-Si or nc a-Si(p)) at the rear and a-Si(i) + a-Si(n) at the front. All cells with nc-Si layers have SiO_x layers at the interface between a-Si(i) and nc-Si(doped) whereby in the last experimental section also micro doping of the interfacial SiO_x layers was investigated. As reference (REF) an SHJ device with a-Si(i) + a-S(n) at the front and a-Si(i) + a-S(p) at the rear is defined. The sketches of the device structures are depicted in Figure 1(A)-(C). The thickness of the doped nc-Si layer (n and p) was in the range of approx. 25 nm. The thickness of the doped a-Si layers is 8 nm for a-Si(n) and 18 nm for a-Si(p). The cells were finalized by sputtered ITO, industrial screen-printing metallization followed by I-V measurements (full area measurement, black non-reflecting chuck).

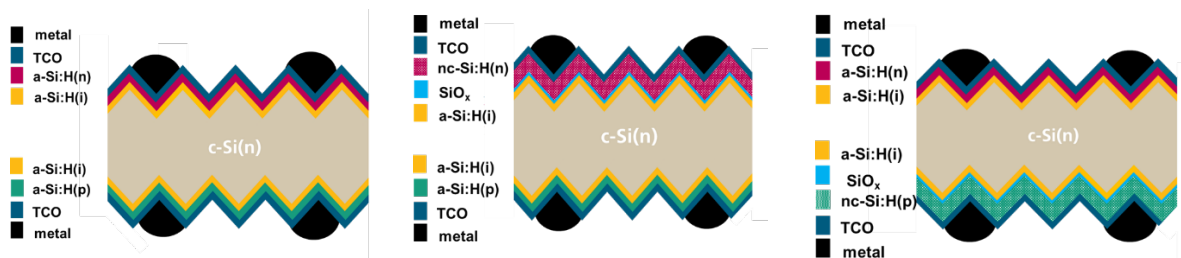


Figure 1(A). SHJ REF device structure with a-Si layers at the front and rear.

Figure 1(B). SHJ device structure with interfacial SiO_x and nc-Si(n) at the front and a-Si REF layers at the rear.

Figure 1(C). SHJ device structure with interfacial SiO_x and nc-Si(p) at the rear and a-Si REF layers at the front.

3. Results and Discussion

3.1 Layer Development – Understanding the Engineering Challenges

First, we developed nc-Si(n) and nc-Si(p) layers on test structures. In line with prior investigations and growth models, e.g., from silicon thin film solar cells [7], we observed a pronounced drop in film resistance with layer thickness. The latter is dominated by the onset of nc-Si and hence more conductive film growth on top of an a-Si incubation layer. We also observe the known conductivity difference, i.e., that p-type (green squares) is more challenging to grow than n-type (red diamonds) nc-Si material. Note that all the depositions were performed on an a-Si(i)-coated glass that was either exposed to ambient air during a VB (resulting in a native

SiO_x layer) or received an SiO_x layer by PECVD prior to nc-Si deposition. The case without VB or respectively without SiO_x layer by PECVD no resistance was measurable and a value of 1000 MΩ was chosen arbitrarily.

The sketches in Figure 2 indicate how the nc-Si evolves during growth. Depending on the plasma regime, the growth starts with an a-Si incubation layer (green area without indicated triangular crystallite structure), followed by nucleation of crystallites and cone-like nc-Si structures, and finally columnar growth (upper green area with indicated triangular crystallite structure). Just as for plain a-Si layers, during incubation and nucleation no resistance is measurable until the nc-Si cones become sufficiently close or start to coalesce. At this point efficient lateral conductivity is enabled and a resistance can be measured indicated by resistance values around 1 and below 1 MΩ. The onset of nucleation strongly depends on the deposition regime and the surface morphology of the substrate. Ideally nucleation would start immediately, yet this is difficult to achieve if the requirement of pristine passivation is to be met. An ultra-thin SiO_x layer at the a-Si(i) surface can help to reduce the incubation layer thickness and protect the a-Si(i) layer from the harsh deposition conditions.

Hence, we investigated the influence of a plasma (PECVD) SiO_x layer to accelerate nc-Si nucleation. To this end a-Si(i)-coated glass was exposed to SiO_x plasma for 0–15 s (without VB) and coated with approx. 25-30 nm of nc-Si(p) (constant plasma conditions). In Figure 2 (right side) the green/white stars indicate the resistance values obtained. Starting at the top (no SiO_x) where no resistance was measurable due to inefficient nucleation (indicated by a resistance value of 1000 mΩ), the positive effect of the PECVD SiO_x is clearly visible as the resistance decreases with deposition time to resistance values below 1 mΩ.

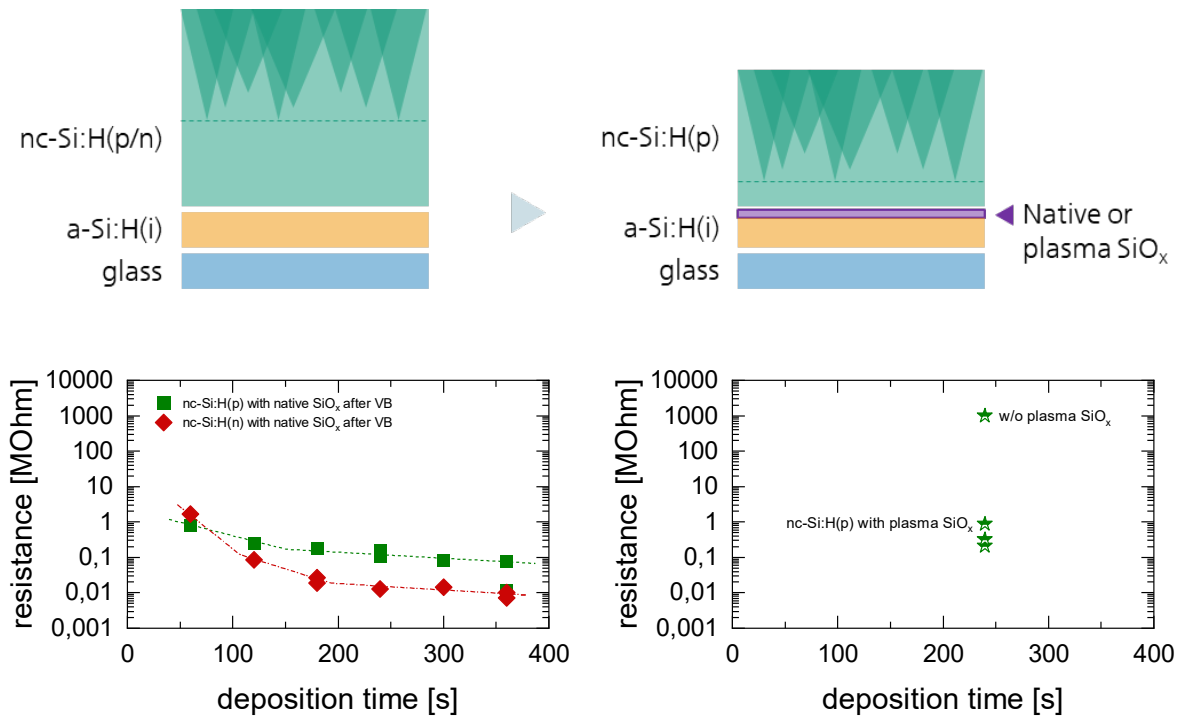


Figure 2. Schematic of the resistance test-structures indicating the nc-Si nucleation in dependence of the presence of an interfacial SiO_x (top) and resistance data for nc-Si(n) and nc-Si(p) layers with native SiO_x after VB (full symbols, down left), or w/o and with a plasma SiO_x layer prior to nc-Si(p) deposition (stars, down right).

3.2 Implementation into Cells

Implementation nc-Si(n)

Implementing nc-Si(n) into cells (see device schematic Figure 1 (B)) leads to the results summarized in Figure 3. In the first column (A) we see a drastic effect for the group w/o vacuum break and therefore with no SiO_x layer in-between a-Si(i) and nc-Si(n) front side layer deposition -see group "no VB" in Figure 3. Without any SiO_x layer present at the interface, either from a VB or PECVD, the cells perform poorly since no proper electron-selectivity is provided by the front contact. This is linked to the fact that the layers are not crystalline and electron-conductive enough and to a strong degradation of the passivating layer. The latter is caused by the harsh deposition conditions of the nc-Si(n) layers resulting in de-passivation of the a-Si/c-Si interface. The presence of a SiO_x layer mitigates this de-passivation. Applying a VB after a-Si(i), prior to nc-Si(n) deposition, the cell performance is comparable to the reference (REF, see device schematic Figure 1(A)) cells using the more optimized a-Si(n) layers. We reproduced the same benefit of a SiO_x layer by varying the SiO_x thicknesses (by varying the deposition times for a CO₂ concentration of 5%) (Figure 3, column (B)) or different CO₂ concentrations for a deposition time of 5 s (Figure 3, column (C)) in the same chamber directly before nc-Si(n) deposition. The percentage of the CO₂ corresponds to its concentration in the SiH₄/H₂/CO₂ gas mixture. It is clearly seen that a treatment time of 2–5 s improves the FF compared to the case without SiO_x. However, beyond 5 s a drop in FF and an overall loss in conversion efficiency is observed. From ellipsometry results we obtained SiO_x layer thicknesses between 0.4 nm at 2 s and 2 nm at 15 s. Hence, we expected an engineering trade-off between sufficiently thick SiO_x for efficient nucleation and sufficiently thin SiO_x for efficient charge carrier transport. Column C indicates that the CO₂ concentration in the gas mix adds another degree of freedom for process tuning and should be chosen high enough. So far, we obtained our champion nc-Si(n) cell with an efficiency of 23% (M2, full area measurement, black non-reflecting chuck). We achieved higher FF values while V_{oc} and J_{sc} were comparable to our reference. Further work will focus on boosting the J_{sc} and hence efficiency by applying ultra-thin nc-Si layers. The layer thickness of the actual nc-Si(n) layers was 25 nm.

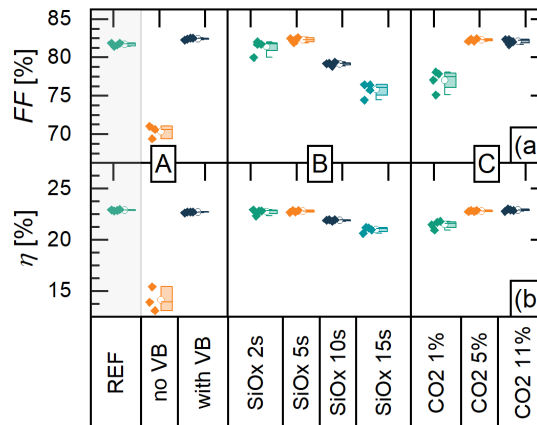


Figure 3. Cell results obtained with **nc-Si(n) layers** at the front, with various SiO_x layers present at the a-Si:H(i) interface. (A) VB, (B) PECVD SiO_x, variation in deposition time for 5% CO₂ content and (C) PECVD SiO_x, variation in CO₂ content in the gas mix for 5 s deposition time.

Implementation nc-Si(p), interfacial SiO_x based on VB

In the second part of this work nc-Si(p) layers were implemented on the rear side of SHJ cells (see device schematic Figure 1 (C)). The front side was prepared according to our standard process recipe for an a-Si(i)-a-Si(n) stack. To investigate the benefits of nc-Si(p) layers for bifacial applications, the cells were illuminated through the front (FS) and rear (RS) side during

IV measurement. The cell performance is reported in Figure 4 for varying nc-Si(p) thickness (thickness nc-Si(p): A and B, $A < B$) and T_{dep} from 180°C to 140°C. All nc-Si(p) layers were deposited after a VB resulting in an interfacial SiO_x layer. Compared to the all-a-Si reference (REF, Figure 1 (A)) with ~18 nm a-Si(p) thickness, nc-Si(p) films of ~25 nm thickness show almost 2 mA/cm² higher J_{sc} due to much better blue response when illuminated from the RS (Figure 4, right side) (through the p-layer). The FF clearly increases towards thicker layers deposited at lower T (140°C) associated to a drop in series resistance. As stated before, the thicker the nc-Si layer, the more crystalline and hence the higher the gains from their beneficial properties. Unlike for n-type layers, series resistance and FF were not yet on pair in this experiment with or better than the reference. Our best cell with nc-Si(p) on the rear (Figure 1 (C)) reached an efficiency of 22% (M2, full area measurement, black non-reflecting chuck).

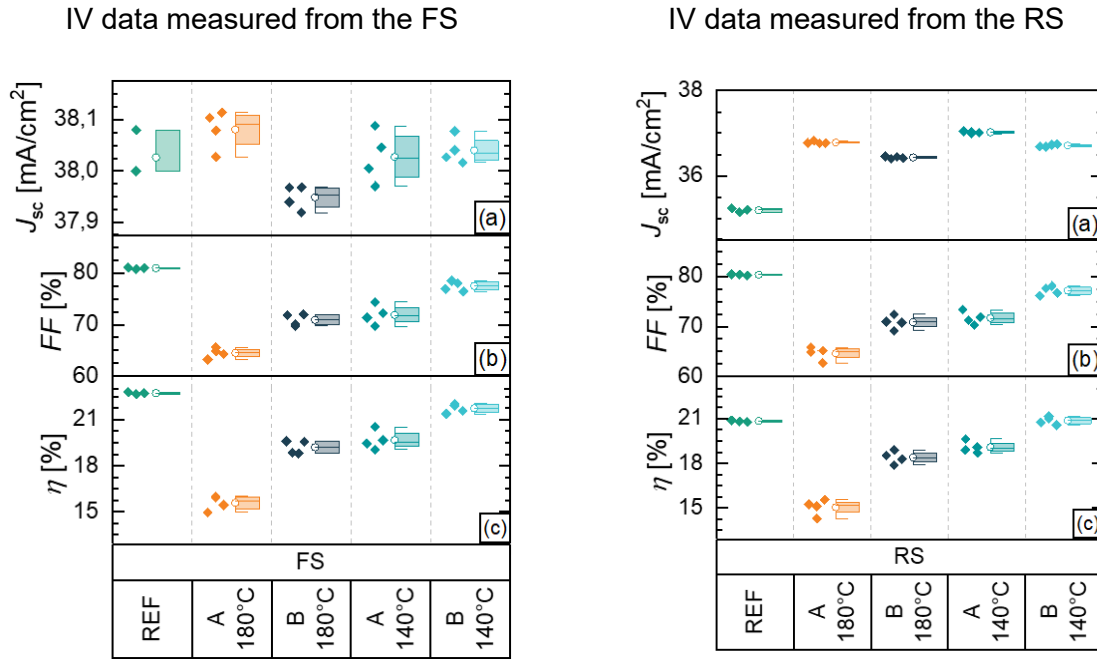


Figure 4. Cell results obtained with **nc-Si(p) layers** of different thicknesses (A and B, where $A < B$) at 180°C or 140°C by alternating deposition and H_2 treatment (layer-by-layer). The nc-Si(p) layers were deposited on the rear side of our SHJ solar cells (see schematic Figure 1 (C)). The cells were illuminated for IV measurement either from the front (FS) or rear (RS).

Implementation nc-Si(p), interfacial SiO_x based PECVD treatment

Depositing the nc-Si(p) layers by continuous plasma and applying a SiO_x PECVD treatment of varying time (2, 5 and 10 s) with varying micro-doping concentration (*p and **p) shows similar as for nc-Si(n) layers that for 5 s high V_{OC} values as for the REF (a-Si(p)) and improved FF can be obtained. The FF values of the nc-Si(p) based cells (schematic Figure 1 (C)) are still below those of the REF (schematic Figure 1 (A)) but have potential to be further improved. J_{SC} values of the nc-Si(p) cells for 5 s SiO_x treatment are slightly higher as for the REF and increase by the implementation of micro-doping with increasing concentration (indicated by *p and **p). Longer deposition time of 10 s (light green group) leads to an SiO_x layer which is too thick for efficient charge carrier transport expressed in a significant lower FF. Implementing a micro-doped SiO_x layer prior nc-Si(p) resulted in a champion efficiency of 23.1% (M2, full area measurement, black non-reflecting chuck) approaching the performance of our a-Si(p) based reference cells. (Figure 5).

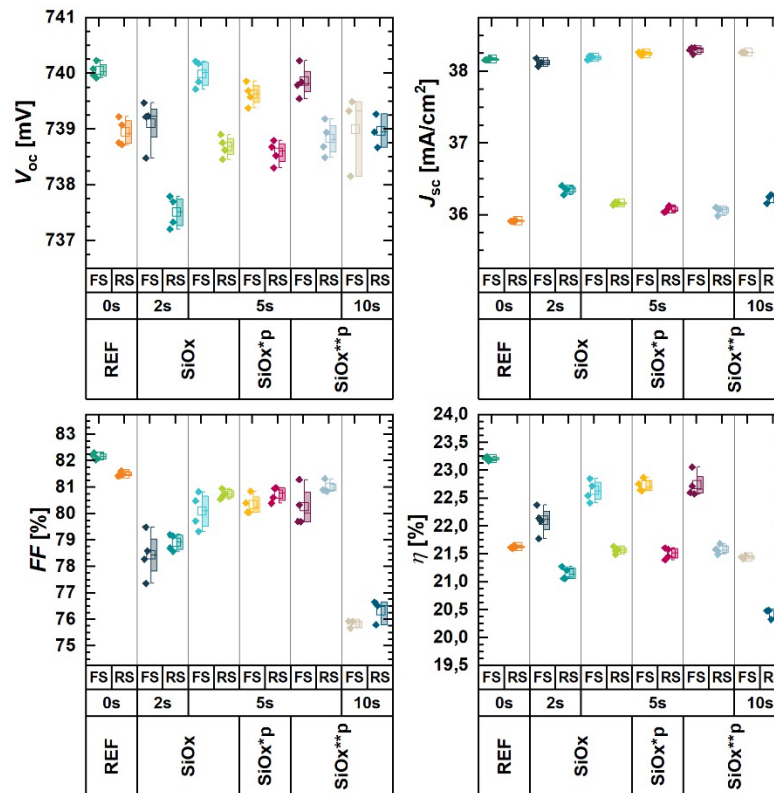


Figure 5. Cell results obtained with **nc-Si(p) layers** deposited by continuous plasma and applying a SiO_x PECVD treatment of varying time (2, 5 and 10 s) with varying micro-doping concentration (*p and **p).

4. Summary and Conclusion

We successfully developed nc-Si(n and p) layers and identified engineering challenges for their application in SHJ solar cells. We found that nc-Si deposition at 140°C and an ultra-thin SiO_x layer (induced by VB or PECVD) helps to accelerate nucleation and improve layer quality. Furthermore, for the PECVD deposition regime used here, an oxide layer at the interface of the a-Si(i) and nc-Si layers also protects the a-Si(i) layer from plasma-induced damage. Implementing a micro-doped SiO_x layer prior nc-Si(p) deposition enables further performance improvements. We obtained conversion efficiencies as high as 23% for nc-Si(n) (front) and 23.1% for nc-Si(p) (rear). The nc-Si based SHJ cells are closing in on our current baseline despite the higher layer thickness, yet further optimization is ongoing.

Data availability statement

The data supporting the results of this contribution are available upon reasonable request from the corresponding author.

Author contributions

Anamaria Steinmetz: Conceptualization, Data curation, Investigation, Visualization, Roles/Writing – original draft, funding acquisition. Johannes Seif Conceptualization, Data curation, Investigation, Visualization, Roles/Writing – original draft. Ibrahim Koc: Investigation,

Resources. Ioan Voicu Vulcanean: Investigation, Data curation, Resources. Dilara Kurt: Resources. Sebastian Pingel: Data curation, Resources Writing – review & editing. Martin Bivour: Supervision, Writing – review & editing.

Competing interests

The authors declare no competing interests.

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