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Cutting Indium Usage by 60% in SHJ-Modules Maintaining High Efficiency

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Abstract. In this work the impact of reducing the Indium consumption for SHJ cells and modules is investigated. Optical simulations show that thinner Indium Tin Oxide (ITO) layers can be used on module level with minor reflection losses while on cell level losses are more severe. For extremely thin ITO layers with a thickness of 7-28 nm on texture a dielectric layer is necessary to maintain / improve the J_{SC} level on both cell and module levels. Results (i) on solar cells (Transfer Length Method - TLM) for lateral resistance and (ii) on shunt structures for vertical electrical resistance showed that there is significant improvement potential if the doping of the layers is adapted parallel to thickness reduction. Solar cell samples with 60% reduced ITO layer thickness on front and rear sides show a similar series resistance level as the 70 nm reference but lower J_{SC}. Optical simulation showed that module integration will recover most of the lost J_{SC} resulting in an expected 0.5%$_{abs.}$ efficiency loss for samples with total (front & rear side) 60% less Indium without adding any process steps. Applying an additional dielectric film enables 80% Indium reduction on the front side with J_{SC} gain on cell level and similar J_{SC} on module level compared to the ITO with reference thickness.

Keywords: Silicon Heterojunction; Indium; Transparent Conductive Oxide

1. Introduction

For silicon heterojunction solar cells (SHJ) the largest challenge is currently the consumption of scarce materials in the production that are critical for the technology to enter the TW market [1], [2], [3]. The following materials: Silver (Ag), Indium (In) and Bismuth (Bi) are the most relevant. The approach of this work to use less In in SHJ cells is to reduce the Indium-Tin-Oxide (ITO) thickness $d_{ITO,txt}$ [4], [5], [6], [7]. The ITO layer acts as transparent conductive oxide (TCO) on front and rear sides (FS/RS) of the SHJ cell. To compensate for increasing sheet resistance R_{sh} the effect of increasing the doping N_e of the thinner layer by varying the relative O_2 flow during physical vapor deposition (PVD) is investigated. Besides the effect of $d_{ITO,txt}$ and N_e on the R_{sh} also the effect on the contact resistivities (i) between metal and ITO $\rho_{c,ITO,metal}$ as well as (ii) the FS stack consisting of the c-Si/a-Si:H(i)/a-Si:H(n)/ITO $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ [8], starting with the c-Si a-Si:H interface and finishing with the ITO bulk layer, is investigated. To understand about the differences in transparency of the TCO layers optical simulations were performed for the different cell and module scenarios with and without dielectric layer. The additional dielectric layer based on Al_2O_3 is applied to compensate for optical losses of thin ITO layers [4], [5].

2. Simulation of the short circuit current density potential

To investigate the impact of FS ITO layer properties on the optics of a SHJ cell the online tool OPAL 2 from PV Lighthouse [9] was used to simulate four different scenarios for the non-metallized cell stack: (i) with air as interface, (ii) with glass as interface, (iii) covered by a dielectric layer with air as interface and (iv) as (iii) with glass interface, as shown in Fig. 1. The simulated device stack consists of c-Si wafer as a base covered by a stack of 6 nm intrinsic and 6 nm n-doped a-Si:H layer and a ITO layer with varied doping (N_e from 0.17×10^{20} to 4.9×10^{20} cm^{-3}) and thickness ($d_{ITO,txt}$ from 0 to 120 nm) on top. For the ITO simulation n and k parameters from [10] available in OPAL 2 [9] for a sputtered ITO film were used. The additional dielectric layer in scenario (iii) and (iv) is applied on top of ITO and metallization to reduce the optical losses due to increased reflection of samples with thin ITO layers. The dielectric layer thickness is optimized to maximize the sample's short circuit current potential: $J_{SC,pot}$ for each scenario and $d_{ITO,txt}$.

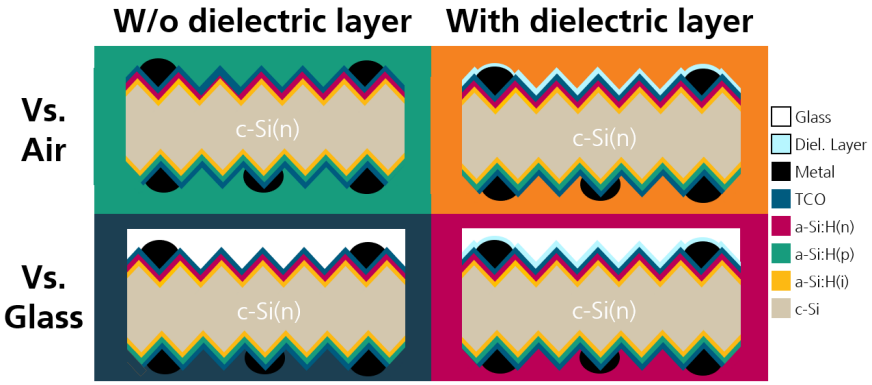


Figure 1. *The four cell / module scenarios.*

3. Experimental

3.1 Symmetrically metallized solar cells and shunt structures

To access the impact on the electrical parameters when changing the ITO properties rear emitter SHJ solar cells and shunt structures for the high-low FS contact were produced. Both sample structures are shown in the Fig. 2 below.

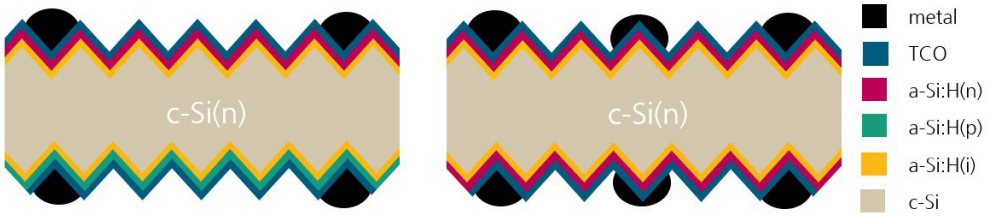


Figure 2. *Structures of SHJ cells and shunt structures.*

Both processes started with a cleaned and textured c-Si(n) wafer (base resistivity ρ_{base} ~ 1 Ωcm) with d_W ~ 165 µm thickness. The wafer surface was passivated by a stack of intrinsic and doped a-Si:H layers deposited by an OCTOPUS 2 PECVD tool from Indeotec. For the solar cells an a-Si:H(p) layer was deposited on the rear side (RS) to form the emitter while a-Si:H(n) is deposited on the FS. In case of the shunt structures the a-Si:H(n) was deposited on both sides symmetrically. After PECVD followed the ITO deposition with a Von Ardenne SCALA PVD tool equipped with a 97/3 rotary ITO target. Depositions were done at industry relevant speed at a power of 4.4 kW. For the SHJ cells on either FS or RS the reference ITO

layer was deposited while on the opposing side the ITO layer was varied in terms of thickness ($d_{ITO,txt}$ from 7 to 70 nm) and doping (N_e from 0.25 to 4.0x10^{20}cm^{-3}). For the shunt structures the varied ITO layers were deposited symmetrically on RS and FS. Subsequent as a last step followed metallization of the samples. The solar cells were symmetrically metallized on an ASYS Ekra screen printing line applying a fine line screen with an opening w_N of 20 µm, resulting in printed width w_F of 30.6 µm ± 2.2 µm and a pitch p_F of 1.3 mm while the shunt structures were metallized with a narrower p_F = 0.65 mm and wider opening w_N = 40 µm (w_F about 51 µm) to keep the resistive losses due to lateral transport in the ITO and at the ITO-metal contact low. In Fig 3. the process of the cell production is documented.

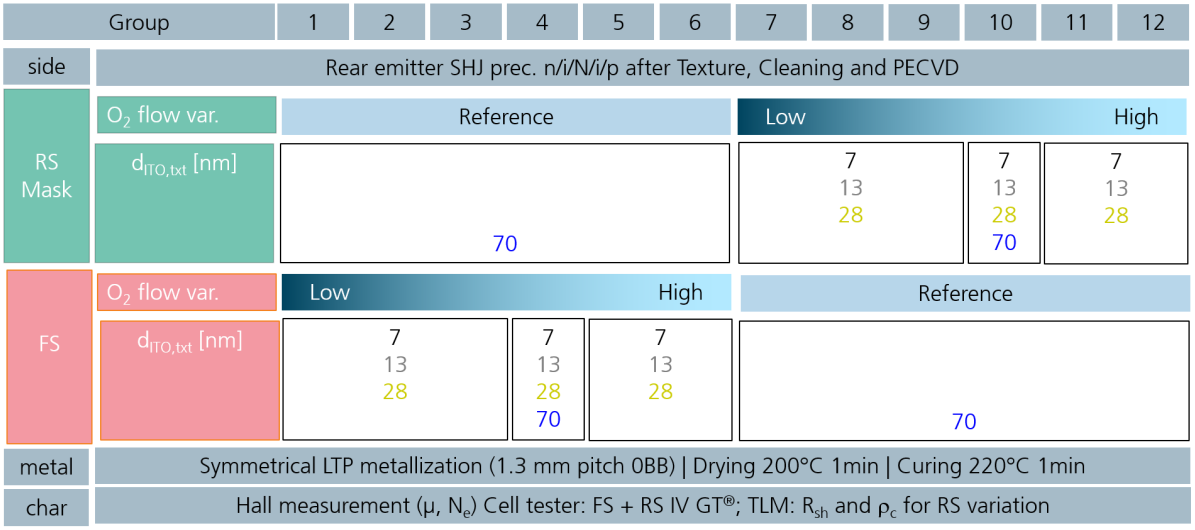


Figure 3. *Process flow for solar cell production.*

Both cells and shunt structures were then characterized in a HALM IV cell tester equipped with a GridTouch® contacting unit. For cells the complete set of IV parameters was extracted while for the shunt structures only the shunt resistance R_P was extracted. The R_P is the base to determine the contact resistivity of the layer stack c-Si/a-Si/ITO $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ according to equation (1) by subtracting the wafer bulk contribution, dividing by a factor of 2 and finally correcting for the ITO-metal contact $\rho_{c,ITO,metal}$ that is used while taking into account the metallized area fraction A_M. Whereas the corrections for wafer are significant, the metal ITO contact correction shows only a minor impact due to the high A_M applied for the shunt structures.

$$\rho_{c,c-Si,a-Si,ITO} = \frac{R_P - \rho_{base} \cdot d_w}{2} - A_M \cdot \rho_{c,ITO,metal} \quad (1)$$

To access the $\rho_{c,ITO,metal}$ in the equation above and the R_{sh} of the different ITO layers TLM measurements were done on the emitter side of SHJ cells with varied RS ITO. To verify the results from the optical simulations, solar cell samples from the reference group 4 with varied $d_{ITO,txt}$ for a fixed O_2 flow received a thermal ALD Al_2O_3 layer on top of ITO and metal and were measured again after the deposition. All ITO layers with different thicknesses and doping were also deposited on flat glass substrates and then characterized with a Hall setup. The parameters doping N_e and mobility μ were extracted.

4. Results

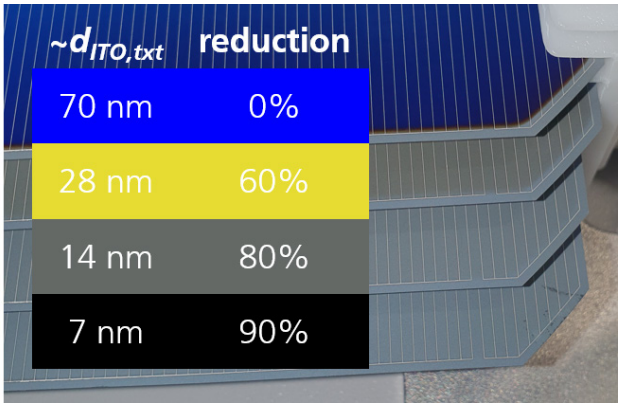


Figure 4. *Photo of the thickness variation applied during ITO deposition.*

Fig. 4 above visualizes the different applied $d_{ITO,txt}$ that are shown for the masked RS ITO of SHJ cells, also the approximate relative $d_{ITO,txt}$ reduction between 60% and 90% compared to the reference with $d_{ITO,txt}$ = 70 nm are mentioned.

4.1 Short circuit current density potential simulation

In Fig. 5 the results of the optical simulation for the $J_{SC,pot}$ that is proportional to the short circuit current density J_{SC} of cells or modules for the four scenarios (Fig. 1) is shown. Reducing the $d_{ITO,txt}$ on the FS of solar cells measured in air (turquoise data points in Fig 5 left) leads to a fast decline of the $J_{SC,pot}$ of the SHJ cell due to the rapidly increasing reflection when moving away from the optimum around $d_{ITO,txt}$ = 70 mm. At the optimum reflection is low because the film has antireflective (AR) properties. For cells encapsulated in modules (blue data) the impact of reduced $d_{ITO,txt}$ is less pronounced (max. J_{SC} loss ~ 1 mA/cm² in the module versus ~ 3 mA/cm² in air). The graph right in Fig. 5 shows the impact of $d_{ITO,txt}$ with an additional dielectric layer on the cell (orange) and module level (red). For moderate doping the $J_{SC,pot}$ is rather independent of $d_{ITO,txt}$ since the dielectric layer thickness is optimized for maximum $J_{SC,pot}$ and then acts as primary AR layer. For moderate N_e highest $J_{SC,pot}$ are found with an optimal $d_{ITO,txt}$ of 30-40 nm for cells and 40-50 nm for modules. For high N_e of 4.9x10^{20} cm^{-3} J_{SC} degrades quickly with increasing $d_{ITO,txt}$ due to increased free carrier absorption (FCA) in the ITO layer.

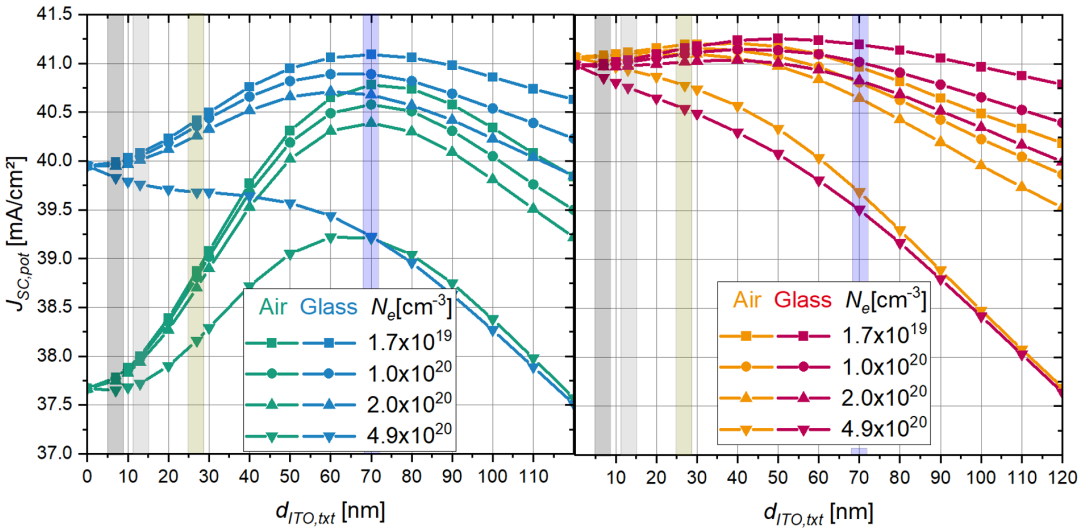


Figure 5. *Simulated short circuit current potential of FS ITO layers with varied thicknesses and doping for the four scenarios: versus air and glass interface (i) for ITO films (left) and (ii) for ITO capped by a dielectric layer (right).*

4.2 Effect of dielectric layer on short circuit current density of SHJ cells

To verify the simulated $J_{SC,pot}$ increase when a dielectric layer is added ontop of ITO layers with varied $d_{ITO,txt}$, samples with varied FS ITO from group 4 where further processed. First, they were measured initially then a dielectric Al_2O_3 layer was deposited on top of the ITO. The dielectric layer thickness was optimized for each $d_{ITO,txt}$ individually for highest $J_{SC,pot}$ in air. Finally, the samples were measured a second time. The difference in J_{SC} was calculated and compared to the $J_{SC,pot}$ increase from the simulations. The result is shown in Fig. 6. The simulation and experimental data show close to perfect agreement. Further IV data is not presented here since the samples with capping were difficult to contact with the busbarless contacting unit and a reduced FF was measured. Similar samples were successfully integrated into modules [11] showing that capping with a dielectric layer is no fundamental problem.

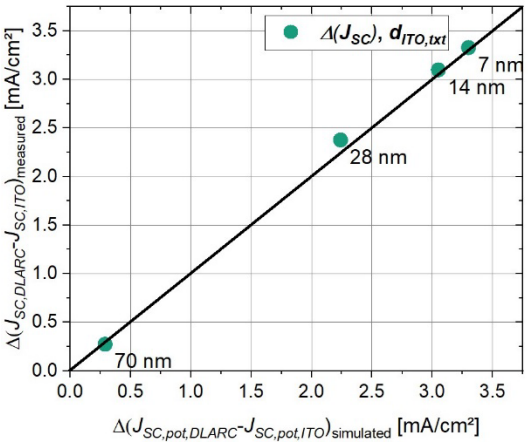
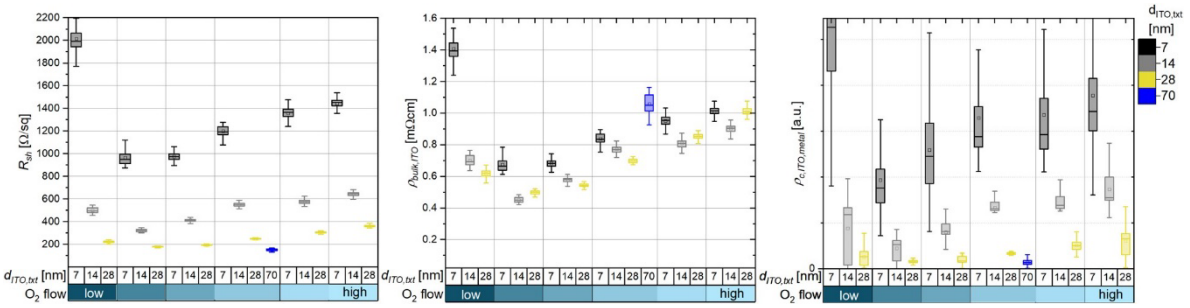


Figure 6. *Comparison of simulated with measured optical gains when an optimized dielectric capping is deposited on an ITO with varied thicknesses.*

4.3 TLM measurements



(a) (b) (c)

Figure 7. *Results from TLM measurement: (a) sheet resistance R_{sh}, (b) sheet bulk resistivity $\rho_{bulk,ITO}$ and (c) contact resistivity ITO-metal $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$.*

The Fig. 7 above shows the extracted R_{sh} from TLM measurements for the different N_e levels and $d_{ITO,txt}$ ranging from 7 nm to 70 nm where corresponding ITO saving range from 0% for the reference to 60, 80 or 90%. For ≥ 80% reduced $d_{ITO,txt}$ the R_{sh} increases quickly. Comparing to the reference layer (blue) shows that for 60% $d_{ITO,txt}$ reduction only a minor increase in R_{sh} is found. Looking at the calculated bulk ITO resistivity $\rho_{bulk,ITO}$ (Fig. 7 b) reveals that for 60% or 80% reduced $d_{ITO,txt}$ and in parallel increased N_e the $\rho_{bulk,ITO}$ is improved by a factor larger than 2. This means that the In utilization can be significantly improved compared to the reference. Contact resistivity $\rho_{c,ITO,metal}$ data, here shown only indicative from linear fits (arbitrary

units) due to inconsistency of the TLM-analysed data gathered with different software versions, show similar trends as R_{sh} and $\rho_{bulk,ITO}$. Reducing the $d_{ITO,txt}$ leads to an increase of the resistance but this can be (partially) compensated by increasing N_e. The TLM analysis shows: in terms of contact to the metal and lateral resistance reducing the $d_{ITO,txt}$ and increasing N_e in parallel leads to improved utilization of In while R_{sh} and $\rho_{c,ITO,metal}$ data are only increased marginally for 60% but more pronounced for 80% or 90% thickness reduction.

4.4 Cell results

A selection of the cell IV parameters is presented in the following figures. The J_{SC} in Fig. 8 shows the effect of increasing reflection of cells measured with air as interface when $d_{ITO,txt}$ on the FS is reduced. The results for the lowest O_2 flow show deviant behaviour due to changed morphology of the ITO-film and is excluded from the discussion. Compared to the simulation (Fig. 5) overall J_{SC} reduction ($d_{ITO,txt}$ 70 nm → 7 nm) is with ~ 3mA/cm² similar. For $d_{ITO,txt}$ = 28 nm an impact of the N_e variation is visible, for 14 nm an insignificant trend is found while for 7 nm a trend is not visible anymore. For the RS only a minor impact of $d_{ITO,txt}$ and N_e was found. In tendency thinner layers on the RS lead to increased J_{SC} measured on the FS. Further also higher N_e led to increased J_{SC}.

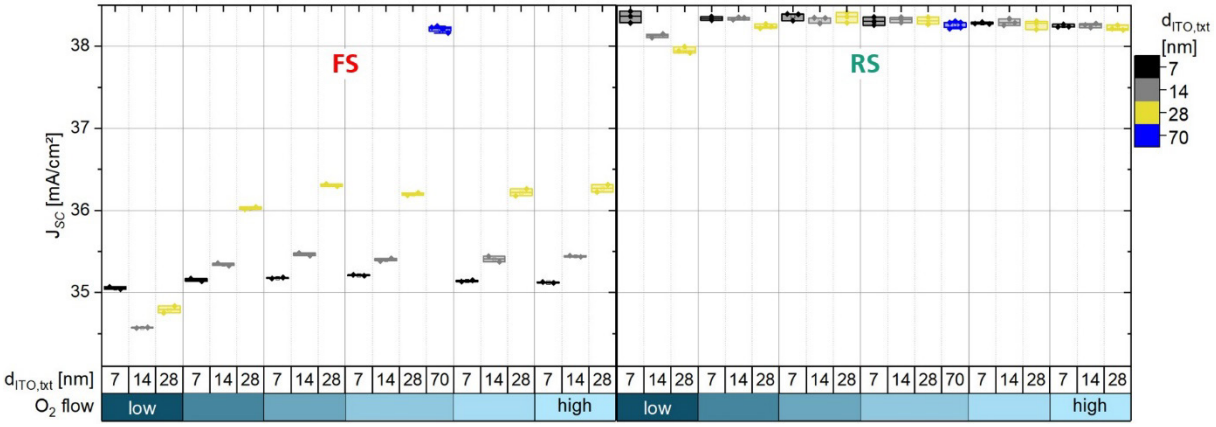


Figure 8. *Cell tester results for the J_{SC} with varied $d_{ITO,txt}$ on cell FS and RS.*

In Fig. 9 the R_S is reduced for a given $d_{ITO,txt}$ when N_e is increased for both FS and RS deposition (besides the excluded group with lowest O_2 flow). Compared to the reference 70 nm ITO on the FS (Fig. 9 left) a 28 nm $d_{ITO,txt}$ shows an overall reduced R_S when N_e is adapted. Even though R_{sh} was increased for 14 nm $d_{ITO,txt}$ the reference R_S level can be maintained. For 7 nm $d_{ITO,txt}$ the R_S level is increased by 0.3 Ωcm² for high N_e. On the RS (Fig. 9 right) the findings are similar to the FS, but the R_S level increases more quickly with reduced $d_{ITO,txt}$ due to the stronger impact of the increasing R_{sh} on the emitter side. For 28 nm the reference R_S level can be kept constant, while for 14 nm or 7 nm it increases by 0.2 or 0.6 Ωcm² respectively when N_e is optimized. The $d_{ITO,txt}$ on the RS can be reduced by 60% without increasing resistive losses. In the considered cases the effect of increased R_{sh} on the RS is pronounced due to the large p_F of 1.3 mm that is typically chosen smaller on the RS to improve η. But overall decreasing the p_F is an option to compensate for higher R_{sh} related losses both on FS and RS.

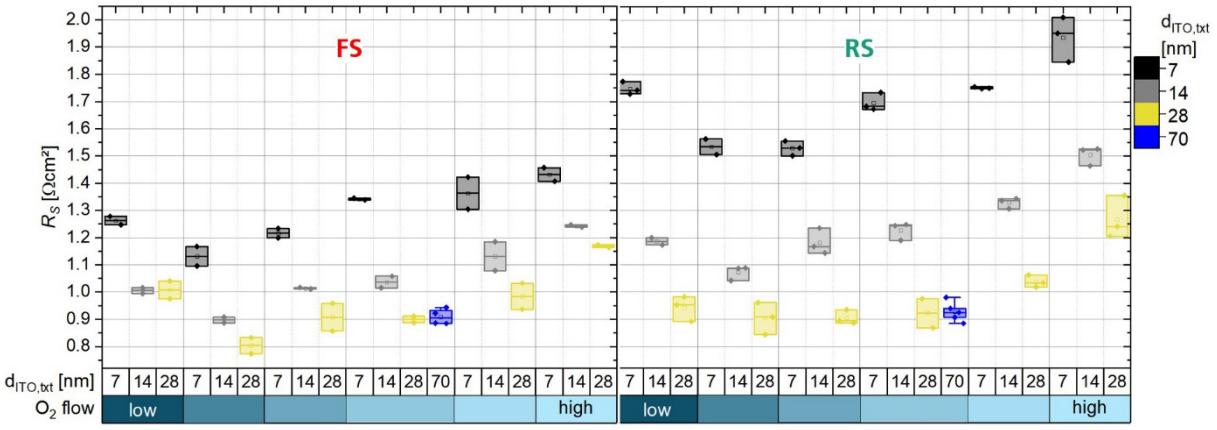


Figure 9. *Cell tester results for the series resistance R_S.*

4.5 Impact of lateral and vertical resistance on the series resistance

In the following Fig. 10, the R_{sh} results from TLM and the $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ determined from shunt structures are plotted versus the R_S of the symmetrically metallized solar cells with single sided ITO variation.

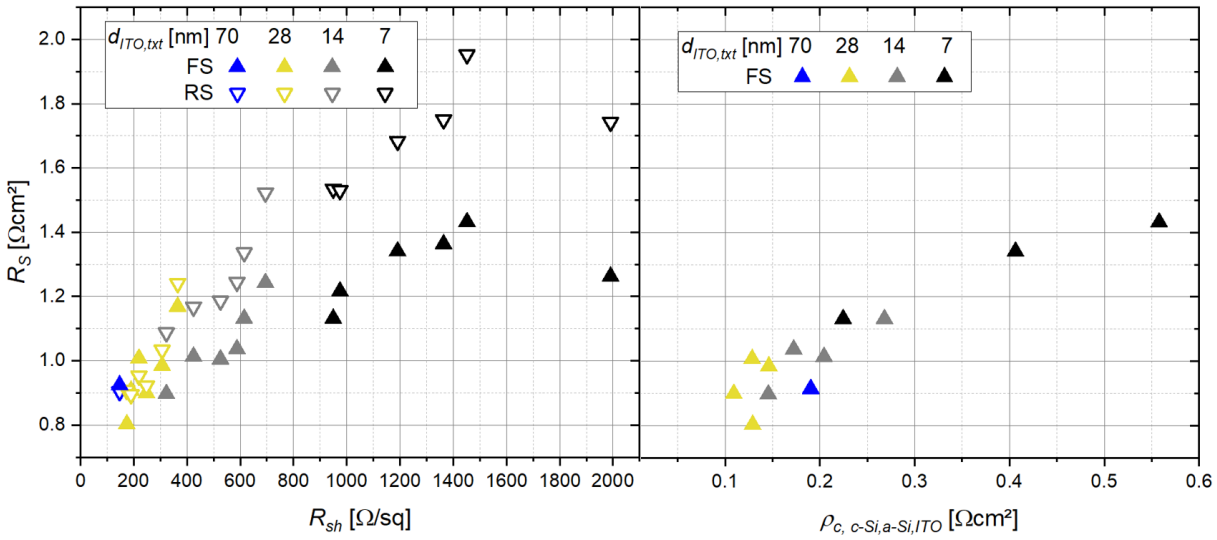


Figure 10. *Scatter plots of R_S versus R_{sh} for ITO variation on cell FS and RS (left) and versus $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ for the cell FS (right).*

As shown in section 3.1 the R_{sh} increases when $d_{ITO,txt}$ is reduced while adapting/increasing N_e leads to decreased R_{sh}. The effect on R_S shown in the left of Fig. 10 is more pronounced on the emitter side of the cells. Low R_S levels are achieved for 28 nm on FS and RS and 14 nm $d_{ITO,txt}$ on the FS. Best cells with 7 nm on the FS and a R_{sh} ~ 1000 Ω/sq led to an R_S increase of 0.2 Ωcm² while on the RS the R_S increase is with 0.6 Ωcm² much more pronounced for the same N_e. The impact of the increased R_{sh} can be compensated by reducing the p_F. Here R_S and shading losses need to be balanced on the FS for optimal η while on the RS shading effects are less relevant. For the FS $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ investigation many samples were broken during the process and only a few samples were finally measured at the cell tester (Fig. 10 right). Compared to the reference a 28 nm ITO leads to improved $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$, adapting the N_e had only a small impact on the $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ but helped for the 14 and 7 nm layers on the FS to keep $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ low. The $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ needs to be reviewed critically in the future since current crowding effects for high R_{sh} values cannot be excluded and potentially led to a substantial effect of the p_F when the current is forced to flow in the wafer and only directly under the contact

finger from the wafer through the layer stack into the metal finger. The data show that even for 7 nm thick layers with $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ ~ 0.23 Ωcm² acceptable R_S increase of 0.2 Ωcm² were achieved on the FS when N_e is increased while without adapting the N_e the R_S increases by 0.45 Ωcm².

4.6 Expected efficiency level

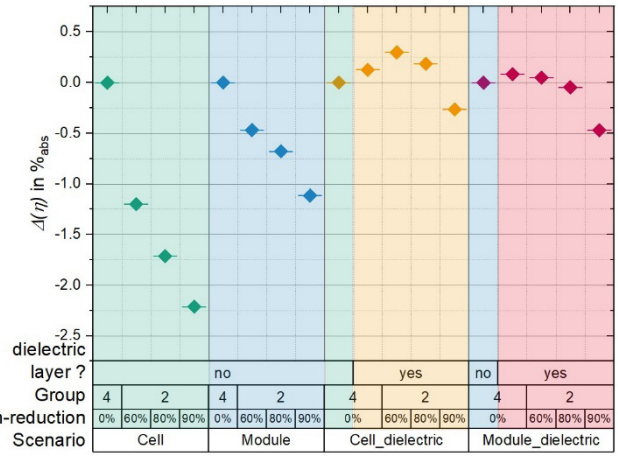


Figure 11. *Expected change in cell and module efficiency for samples with dielectric capping compared to the uncapped reference with variation of the ITO thicknesses on the FS.*

Based on the IV results of the symmetrically metallized solar cells and the simulated change in $J_{SC,pot}$ an expected η-level, see Fig. 11, was roughly calculated. Here the η on cell level for the reference ITO and varied $d_{ITO,txt}$ on the FS with adapted N_e was considered as well as the expected change in J_{SC} according to OPAL 2 simulation (compare Fig. 5 and 6). On cell level reducing $d_{ITO,txt}$ on the FS by 60% or more leads to high η-loss (>1%$_{abs}$). On module level for the 60% $d_{ITO,txt}$ reduction the expected η-loss is 0.5 %$_{abs}$. If an additional dielectric layer is applied on a 28 nm ITO, η is expected to improve on cell level (~0.3%$_{abs}$) compared to the reference ITO without dielectric layer. On module level with a capping layer the η can be maintained or marginally improved. Reducing $d_{ITO,txt}$ by 90% leads to significant losses in all scenarios due to decreasing J_{SC} and high R_S. This investigation does not consider the adaption of the metallization to compensate for an increase in lateral R_{sh} losses by applying a smaller p_F. Here it is expected that the η-optimum shifts to thinner ITO layers as long as the $J_{SC,pot}$ (Fig. 5) is not substantially declining. On the cell RS applying a 28 nm $d_{ITO,txt}$ was possible while keeping the same R_S level. In summary $d_{ITO,txt}$ reduction on both sides by 60% is possible on module level when 0.5 %$_{abs}$ η-loss is considered acceptable. If an additional dielectric layer is applied the FS $d_{ITO,txt}$ reduction can be increased to 80% without scarifying η on both cell and module level.

5. Conclusion and Outlook

Within this work promising ITO layers with reduced $d_{ITO,txt}$ were explored that allow to reduce In-consumption by 60% or more. On the cell RS a 60% reduction was shown to achieve the same R_S level as the 70 nm reference even though the R_{sh} increased, and a large p_F was applied. Since the optics on the RS are less important [10], both for bifacial but especially for mono-facial modules thickness reduction by 60% or more are expected to be applicable without η loss. On the cell FS the R_S level can be improved when going from 70 nm reference to 28 nm but higher reflection leads to η-loss greater than 1%$_{abs}$ on cell and an expected 0.5%$_{abs}$ loss on module level. Adding a dielectric layer on the FS enables η-gains on cell level and similar η-level in modules for 28 nm thick ITO films compared to the reference. Also capped thin ITO layers (14 nm / 80%) are expected to achieve similar η on cell and module

level. Central factors effecting the R_S were explored by TLM and shunt structure measurements. The interplay of both extracted parameters R_{sh} and $\rho_{c,c\text{-}Si,a\text{-}Si,ITO}$ were shown to be useful to describe and understand R_S related effects. It could be shown that the In utilization in terms of $\rho_{bulk,ITO}$ can be substantial improved if $d_{ITO,txt}$ and N_e are both adapted. The process sequence for shunt structures needs more attention in the future. It is planned to investigate current crowding and spreading resistance effects to clarify if the method with a printed grid is reliable also for ITO films with high R_{sh}. For thin ITO layers and additional dielectric layers module integration and module reliability needs to be investigated. Besides the approach of capping thin ITO with a dielectric layer also the simplified approach with a thin In-based TCO capped with In-free TCO is investigated. This allows strong reduction of the In-consumption and simplifies the processing since no extra tool for applying the capping layer is necessary [12], [13].

Data availability statement

The data supporting the results of this contribution are available upon reasonable request from the corresponding author.

Author contributions

Conceptualization: S. Pingel, M. Bivour, A. Steinmetz; Funding acquisition: M. Bivour, A. Steinmetz; Methodology: S. Pingel, A. Krieg, M. Bivour; Project administration: S. Pingel, I. Vulcanean, W. Wolke; Resources: I. Vulcanean, C. Röhnelt, W. Wolke, V. Georgiou-Sarlikiotis; Supervision: A. Steinmetz; Writing – original draft / review & editing: S. Pingel, A. Krieg, M. Bivour, A. Steinmetz

Competing interests

The authors declare that they have no competing interests.

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References

[1] VDMA: ITRPV 14. Edition
[2] Zhang, Yuchao; Kim, Moonyong; Wang, Li; Verlinden, Pierre; Hallam, Brett (2021): Design considerations for multi-terawatt scale manufacturing of existing and future photovoltaic technologies: challenges and opportunities related to silver, indium and bismuth consumption. In Energy Environ. Sci. 14 (11), pp. 5587–5610. DOI: 10.1039/D1EE01814K.
[3] Gervais, Estelle; Herceg, Sina; Nold, Sebastian; Weiß, Karl-Anders (2021): Sustainability strategies for PV: framework, status and needs. In EPJ Photovolt. 12, p. 5. DOI: 10.1051/epjpv/2021005.

[4] Bätzner, D. L.; Papet, P.; Legradic, B.; Lachenal, D.; Kramer, R.; Kössler, T. et al. (2019): 'HJT 2.0' Performance Improvements and Cost Benefits for Silicon Heterojuntion Cell Production. 4 pages / 36th European Photovoltaic Solar Energy Conference and Exhibition; 300-303. DOI: 10.4229/EUPVSEC20192019-2EO.1.3.

[5] Morales-Vilches, Anna B.; Cruz, Alexandros; Pingel, Sebastian; Neubert, Sebastian; Mazzarella, Luana; Meza, Daniel et al. (2019): ITO-Free Silicon Heterojunction Solar Cells With ZnO:Al/SiO 2 Front Electrodes Reaching a Conversion Efficiency of 23%. In IEEE J. Photovoltaics 9 (1), pp. 34–39. DOI: 10.1109/JPHOTOV.2018.2873307.

[6] Can Han; Rudi Santbergen; Max Duffelen; Paul Procel; Yifeng Zhao; Guangtao Yang et al.: Towards bifacial silicon heterojunction solar cells with reduced TCO use, DOI: 10.1002/pip.3550

[7] Jay, Frederic; Gageot, Tristan; Pinoit, Gabriel; Thiriot, Benjamin; Veirman, Jordi; Cabal, Raphael et al. (2022): Reduction in Indium Usage for Silicon Heterojunction Solar Cells in a Short-Term Industrial Perspective. In Sol. RRL, p. 2200598. DOI: 10.1002/solr.202200598.

[8] Luderer, C.; Messmer, C.; Hermle, M.; Bivour, M. (2019): Contact Resistivity of the TCO/a-Si:H/c-Si Heterojunction. 3 pages / 36th European Photovoltaic Solar Energy Conference and Exhibition; 538-540. DOI: 10.4229/EUPVSEC20192019-2DV.1.48.

[9] McIntosh, Keith R.; Baker-Finch, Simeon C. (2012): OPAL 2: Rapid optical simulation of silicon solar cells. In: 2012 38th IEEE Photovoltaic Specialists Conference. 2012 IEEE 38th Photovoltaic Specialists Conference (PVSC). Austin, TX, USA, 03.06.2012 - 08.06.2012: IEEE, pp. 265–271. https://doi.org/10.1109/PVSC.2012.6317616.

[10] Holman, Zachary C.; Filipič, Miha; Descoeudres, Antoine; Wolf, Stefaan de; Smole, Franc; Topič, Marko; Ballif, Christophe (2013): Infrared light management in high-efficiency silicon heterojunction and rear-passivated solar cells. In Journal of Applied Physics 113 (1), Article 013107. DOI: 10.1063/1.4772975.

[11] Heitmann, U.; Tutsch, L.; Rose, A. de; Dreja, D.; Jakob, L.; Elgazzar, R. et al. (2022): Reduction of ITO by a Low-Cost Sprayed TIOx Capping Layer for SHJ Solar Cells. 4 pages / 8th World Conference on Photovoltaic Energy Conversion; 59-62. DOI: 10.4229/WCPEC-82022-1BO.3.3.

[12] Cao Yu; Qiaojiao Zou; Qi Wang; Yu Zhao; Xiaochao Ran; Gangqiang Dong et al.: Silicon solar cell with undoped tin oxide transparent electrode, DOI: 10.1038/s41560-023-01331-7.

[13] Schmid, Philipp; Wolke, Winfried; Nagel, Henning; Tutsch, Leonard; Georgiou-Sarlikiotis, Vasileios; Steinmetz, Anamaria et al. (2023): Reducing Indium Consumption in Silicon Hetero Junction Solar Cells With TCO Stack Systems of ITO and AZO. In IEEE J. Photovoltaics 13 (5), pp. 646–655. DOI: 10.1109/JPHOTOV.2023.3267175.