SiliconPV 2024, 14th International Conference on Crystalline Silicon Photovoltaics
Advanced Manufacturing, Challenges for Industrial Devices
https://doi.org/10.52825/siliconpv.v2i.1317
© Authors. This work is licensed under a Creative Commons Attribution 4.0 International License
Published: 06 Dec. 2024

Patterning by Selective Etching of Poly-Silicon Using a High Etch Rate Single Sided Gaseous Process

Laurent Clochard[1], David Young[2], Mingzhe Yu[3], and Ruy Sebastian Bonilla[3]

[1] Nines Photovoltaics, Synergy Centre, Ireland

[2] National Renewable Energy Laboratory, USA

[3] University of Oxford, UK

*Correspondance: Laurent Clochard, l.clochard@nines-pv.com

Abstract. This paper presents etching process developments using a single-side gaseous etch process based on the thermal reaction of poly-Silicon and the etching gas (molecular fluorine), that results in a high etching selectivity between layers, and a high etching rate. This work was carried out in the context of the development of solar cell architectures beyond PERC and TOPCon, where more sophisticated etching steps are required in order to accurately pattern poly-silicon layers across the wafer surface.

Keywords: TOPCon, Patterning, Etching, Solar Cell, Selectivity, Dry Etching, Gas-Phase Etch

1. Aim and approach

Tunnel oxide passivated contacts (TOPCon) are being introduced in industrial manufacturing in order to increase the solar cell efficiencies beyond PERC cells performances. Typically, to avoid direct contact between the metallization and the silicon, a layer stack of a thin tunnel oxide and a doped poly-Si layers is introduced, effectively reducing charge carrier recombination at the interface (passivation).

The rear contacts of the solar cells are the most straightforward to passivate, by applying a full surface layer stack of an ultra-thin oxide of a few nanometres, topped with a layer of doped amorphous silicon. This is a method that is becoming mainstream in industrial manufacturing. However, applying the same method to the front contact, the full area poly-Si leads to high parasitic absorption of ~ 0.5 mA/cm² per 10 nm poly- Si, and surface passivation degradation for poly-Si layers <10 nm [1]. Therefore, applying a full area poly-Si to the front side result in a net loss.

Figure 1. *TOPCON cells with: a) full area poly-Si on both sides b) localised poly layer on front side*

When the front poly-Si layer is only under the metal contacts (fingers), the efficiency gain is calculated to be up to +0.5% absolute [2] from a Voc increase of about 10mV.

In this work we investigate the patterning of poly-Si using a single sided gas-phase etching process, removing the poly-Si from the unwanted areas. This gaseous etching process, commonly referred as ADE (Atmospheric Dry Etch) has been used previously for texturing applications of multi-crystalline wafer [3], and for the poly-Si wrap-around removal produced by commonly used industrial deposition tools such as low pressure and plasma enhanced chemical vapor deposition tools (LP-CVD and PE-CVD) [4]. A key feature of this gas-phase process is the etch rate it can deliver, at least an order of magnitude higher than commonly used KOH wet etching, that makes it highly suitable for industrial processing. The rational to use a dry etch process is to reduce water consumption of the etching process steps. Considering the enormous size of modern solar cells giga-factories and the extra etching steps required for advanced cell architectures such as TOPCon, it is becoming critical to reduce their impact on local water resources. This process also uses elemental Fluorine as the etching gas, with no global warming potential. This makes a strong differentiation from typical etching gas used in the semiconductor industry that are green house gases with very high global warming potential (GWP) such as SF6 (17,200 times 100 year GWP kg CO2 equivalent) and NF3 (22,800 GWP), and are unsustainable for industrial use.

The validation of the suitability of the process was split in three building blocks: first the ideal etch process needs to demonstrate a good selectivity between layers, i.e. the layers used to protect the useful areas versus the layers to be etched. Second, the process window needs to allow for a good etch stop control, in order to minimize the impact on the underlayers. Finally, the resulting etched surface needs to be suitable for passivation, using standard layers compatible with standards used in the industry.

2. Experimental

For this set of experiments, p-type Cz wafers of M0 and M2 sizes were used to characterise the etch rate of various deposited layers. The wafers kept in a shipping wafer box, stacked on each other requires a short pre-clean to remove organic contamination and achieve a more uniform result. They are typically pre-cleaned in a 5%HF solution for 1 minutes, followed by 5minutes D.I. rinsing, and 10minutes drying in 95%Nitrogen at 80degC, before being processed through an Atmospheric Dry Etching reactor (ADE).

Figure 2. *Atmospheric Dry Etch reactor schematic and commercial version*

The reactor temperature is set at 220 degC. The etch rate is directly affected by temperature and gas concentration. The overall gas flow setting affects the efficiency of the process, i.e. utilisation rate of the gas. The wafers are weighted before and after the process, with a 1mg balance accuracy. The average etched thickness across the wafer surface can be calculated from the measured weight loss, the wafer dimensions, and the theoretical density of the etch materials.

3. Etch selectivity

A variety of layers were deposited on c-Si wafers with flat surfaces after saw damage removal (no texture). The samples were etched in similar process condition. Figure 3 is a graph summarizing the results. The etch rate E_x is the speed of the etching process for a material [nm/min]. The etch selectivity is the ratio S of etch rates between materials and defined here as:

$$S = E_x / E_{c_Si} \quad (1)$$

It was found that the etch rate is highly dependent on the nature of the layer. Layers of n-poly Si and i-poly Si have very similar etch rates to c-Si. Dielectric layers such as nitride are much slower to etch. SiC, thick thermal oxides and BSG glass add another order of magnitude to the selectivity and can therefore provide excellent etch stop, as demonstrated in previous publication [4]. It was also found that Boron doped silicon can slow down the etch rate considerably, as it is the case for heavily doped p-poly silicon layers resulting in selectivity of 11 between n-poly and p-poly layers, and to a lesser extend for a typical Boron emitter. Overall, when using ADE, the etch is very selective.

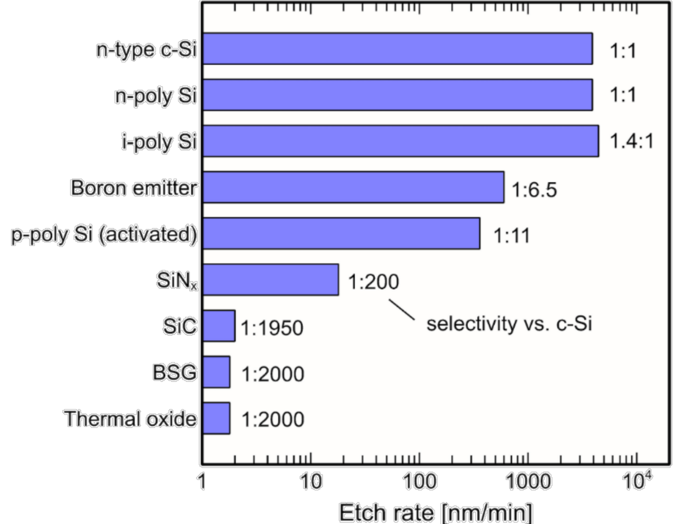

Figure 3*. Etch rate and selectivity of the F2 gas-phase etch toward c-Si for various layer*

4. Etch process window

Here we designed a set of experiments in order to map the process window around the transition between the poly-layer, the tunnel oxide and the crystalline silicon. The samples were symmetrical, textured and deposited on both sides with a stack of a 1.5nm thin oxide and a 200nm layer of intrinsic poly-Si. The etch process parameters were set in order to get a higher accuracy by slowing down the etch rate.

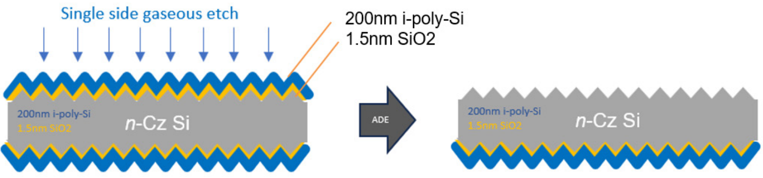

Figure 4. *Schematic of the samples and stack used for the etch process window experiment*

Wafers were processed one at a time, gravimetric measurement was carried out before and after the etch (+/-1mg). The velocity of the wafer passing through the reactor was the main process variable. The etch gas concentration was set to 10% and 1%. To calculate the etch depth in nanometres, a density of 2.329 was assumed for c-Si and 2.285 for the intrinsic poly-Si.

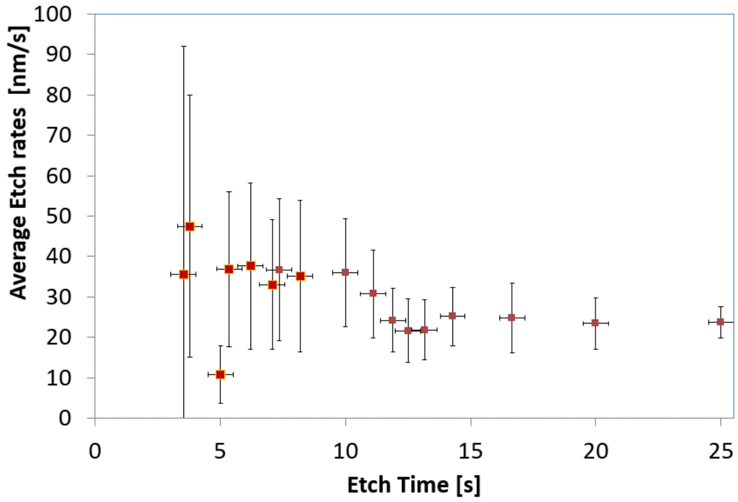

Figure 5. *Time Averaged etch rates vs etch time*

The data obtained show two different etch rates, separated by a transition phase. The thin oxide seems to be slowing down the etch rate. Such a thin <2nm oxide, and somewhat porous layer could not act as a complete etch stop however, and can eventually be overcome by the fluorine etch process, despite the strong etch selectivity of the process toward oxides. The transition can be clearly mapped through the etch rate, and provides process control. The data for short etch time is less reliable as the weight loss is converging toward the accuracy limit of the weighing scale (+/-1mg).

5. Surface passivation preliminary results

A first attempt was made to re-passivate some of the samples from the above paragraph by growing a ~30 nm of Al_2O_3 using ALD, and subjecting the samples to a 60 min FGA. Four samples were selected for short, medium and long etch times. They were then characterised using Sinton data, as per Fig. 6.

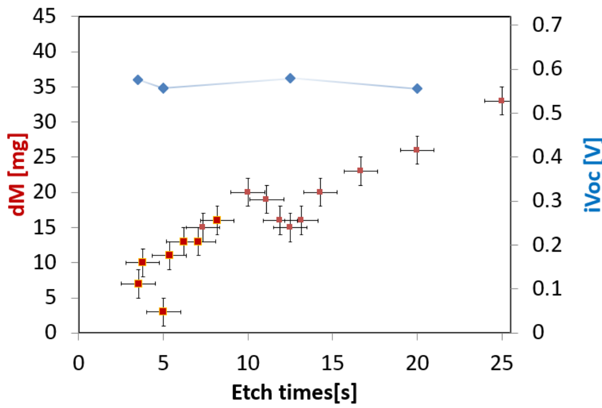

Figure 6. *iVoc results after passivation*

The iVoc results hovered around 570 mV, significantly lower than the initial 710 mV reference. The reference was obtained using the initial precursor, followed by 850degC annealing, ALD AlOx deposition and FGA). Note that the samples had to be dipped in HF before passivation, hence removing any of the tunnel oxide that would have survived the etch. There are open questions remaining around the suitability of the single layer passivation stack ; the experiments would probably benefit from an FGA variation, and possibly a full passivation stack including SiNx.The optimal passivation stack selection would also depend on the degree of etching of each sample, i.e. weather there is some poly layer or oxide remaining. Overall, and without having access to further investigation, this first passivation result is rather inconclusive.

Another attempt was made with a second set of samples. This time the stack was slightly different, depositing 325nm of n-poly-Si on top of a 1.5nm tunnel oxide, and the layers were masked (with a proprietary process) before etching with the single side ADE process.

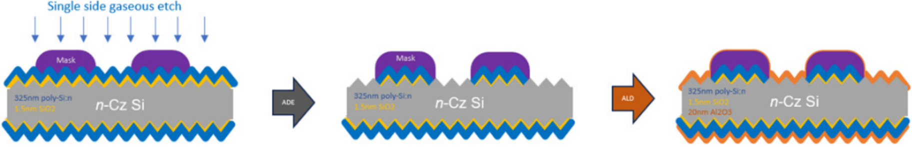

Figure 7. *Schematic of the process steps for the Second set of samples*

The samples were then passivated after cleaning by UV/O3 and an HF dip variation, by depositing a 20nm AlOx layer by ALD on both sides, and annealing at 400C on a hotplate with variations from 2 to 20 minutes. PL imaging was realised after metallization, in order to compare to an industrial TOPCon cell in a qualitative manner.

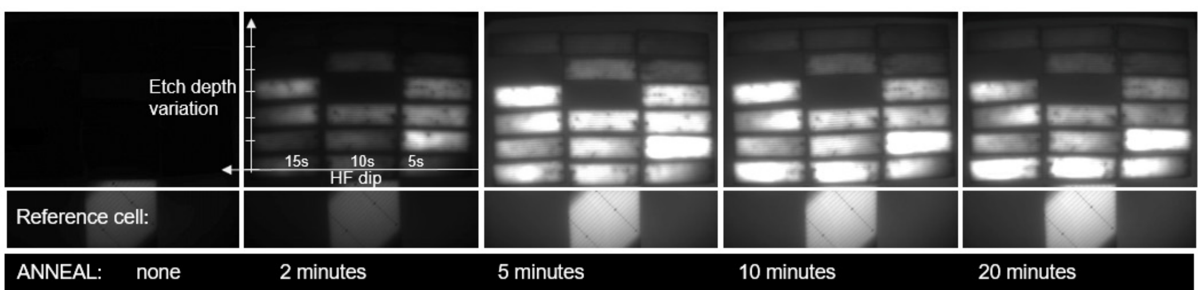

Figure 8. *Photoluminescance (PL) measurement results, with variations of 1) Etch depth (vertical), 2) Anneal time (Horizontal left to right) 3) HF dip duration (Horizontal small axis rigth to left)*

The hotplate anneal required at least 5 minutes, and did not show much improvement beyond this. A Shorter HF dip also seemed to be more favourable.

For the samples that had a 5 second HF dip and 5 minutes anneal, SEM imaging was carried out to inspect the surface, for various etch duration. Fig. 9 shows the various conditions, from under-etching showing left over poly-Si, to over-etching were the pyramid texture disappears.

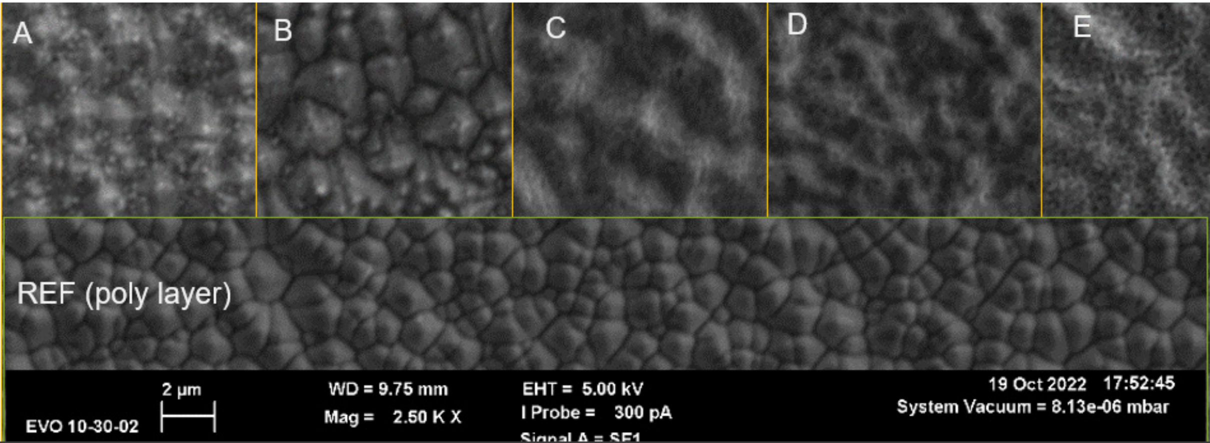

Figure 9. *SEM of the surface after etching after various etching time: (A)8s B)16s C) 28 D) 30s E) 32s*

6. Conclusion

Several building blocks have been investigated, regarding the use of a gas-phase single sided dry etching process suitability for the selective etching of poly-Si layer. A strong selectivity has been demonstrated. The passivation of the post etch surface results are inconclusive and point out the necessity for further, more detailed experiments.

Data availability statement

The data this article is restricted (third-party data).

Underlying and related material

None.

Author contributions

Laurent Clochard: Conceptualization, data curation, writing, investigation, resources

David Young: investigation, resources

Mingzhe Yu: investigation

Ruy Sebastian Bonilla: Resources

Competing interests

The authors declare that they have no competing interests.

Acknowledgement

If you want to acknowledge persons or institutions you can do so here.

References

[1] F. Feldmann, C. Reichel, R. Müller and M. Hermle, "Si solar cells with top/rear poly-Si contacts," 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, USA, 2016, pp. 2421-2424, https://doi.org/10.1109/PVSC.2016.7750076.

[2] J. Stuckelberger, et al., EUPVSEC (2020) Industrial Solar Cells Featuring Carrier Selective Front Contacts.

[3] B. Kafle, T. Freund, S. Werner, J. Schon, A. Lorenz, A. Wolf, L. Clochard, E. Duffy, P. Saint-Cast, M. Hofmann, J. Rentsch, „On the Nature of Emitter Diffusion and Screen-Printing Contact Formation on Nanostructured Silicon Surfaces," IEEE J. Photovoltaics. 2017 7, 136, https://doi.org/10.1109/JPHOTOV.2016.2626921.

[4] Kafle, B., Mack, S., Teßmann, C., Bashardoust, S., Clochard, L., Duffy, E., Wolf, A., Hofmann, M. and Rentsch, J. (2022), Atmospheric Pressure Dry Etching of Polysilicon Layers for Highly Reverse Bias-Stable TOPCon Solar Cells. Sol. RRL, 6: 2100481. https://doi.org/10.1002/solr.202100481.