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How to Combine SHJ Cell-Edge Passivation and Module Reliability?

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Abstract. The use of cut-cells in most of the current modules is now the norm to maximise the final product performances. But the integration of such new cell configurations also comes with new challenges, especially if small cell size dimensions such as shingle are considered. Indeed, specific edge passivation processes are often used to recover for the cut-cell losses. Alumina Oxide or Polymer deposition are the most studied approaches, with in general promising benefits proven at cell level. However, only few communications after module integration are available, in particular about the impact of these additional layers on final module reliability. We show for example that it is crucial to avoid direct deposition of AlO_X over the cell metal pattern in the future interconnection area, as TC (Thermal Cycling) resilience of such modules is clearly degraded. Proper edge localization of the AlO_X layer is needed to recover the initial reliability behaviour. To preserve the interconnection quality, three different approaches are investigated: (1) edge localisation of the layer by wafer stacking during deposition (2) introduction of adapted copper plating solutions allowing metal growth through the passivation layer (3) edge passivation process directly applied on final strings just before lamination.

Keywords: Cut-Cell, Edge Passivation, Shingle, Reliability

1. Introduction

Silicon Heterojunction is one of the most attractive technology, combining high power and a simple fabrication process flow. However, it is recently facing new challenges, as module integration scheme is progressively moving towards half-cell or even shingle interconnection. Indeed, as presented in previous publications [1], [2], quite severe performance losses are observed when such SHJ cells are cut, linked to the generation of an unpassivated edge. Several research activities on cut optimization or edge repassivation are conducted, with most institutes/companies reporting final cell efficiencies close to the initial full-cell performances [3], [4]. Therefore, the growing interest of moving towards these new module configurations must be properly evaluated, both in terms of module final performances, but also in terms of long-term module stability and reliability. Such analysis has already been initiated in [1] for half-cell configuration, but constraints can appear even stronger when a shingle configuration is considered. Indeed, the small stripe configuration combined with its excellent overall reliability (less than 2% relative losses reported in [5] for up to 1000 TC -Thermal Cycling- cycles), makes such interconnect scheme highly sensitive to the specific impact of edge defectivity/edge passivation additional processes. We thus propose for the first time in this abstract to analyze at module level the impact of usual AlO_X based edge-passivation processes generally considered

in the literature. We demonstrate in particular that localization of the new passivation layer out of the interconnection area seems mandatory to preserve the module overall reliability and we propose different technological solutions to simply and successfully achieve this newly identified constraint.

2. Experimental details

The work presented in this abstract has been conducted on shingle Silicon Heterojunction (SHJ) configuration. This cell/module architecture is particularly sensible to cut-edge defectivity/repassivation impact because of the smaller size of the cells, but also due to the specific metallization design, with the interconnect metal busbars located at the very edge of the device. Furthermore, low-temperature ECA-based interconnection strategy is generally considered for shingle module integration, increasing the importance of final cell interfacial optimization to allow good combined adhesion and lowest possible additional resistive contribution. The edge passivation layer explored in this work is a thin Alumina Oxide layer (typically 10 to 15nm thick) generally deposited over the full front surface by low-temperature thermal ALD [3], [6]. Activation of the AlO_X layer is insured by a light soaking anneal step applied to the whole shingle cell [5min, 10 Suns]. SHJ cells used were generated on M2-size CZ wafers in an industrial environment, and integrated in mini-modules (6 or 12-shingle tile) configuration on a commercially available tabber-stringer.

3. Impact of edge-passivation layer on module performances

As already emphasized in the introduction, several studies have already shown significant recovery of performances losses when optimized edge-passivation process is properly applied on cut-cells. But what happens at module level? Several shingle mini-modules have been manufactured, integrating the best SHJ edge-passivated cells produced. We thus show first in Figure 1, that the performance improvements seen at cell level are successfully maintained at module level, demonstrating again the high interest of integrating this new passivation process to enhance the performance of the final modules.

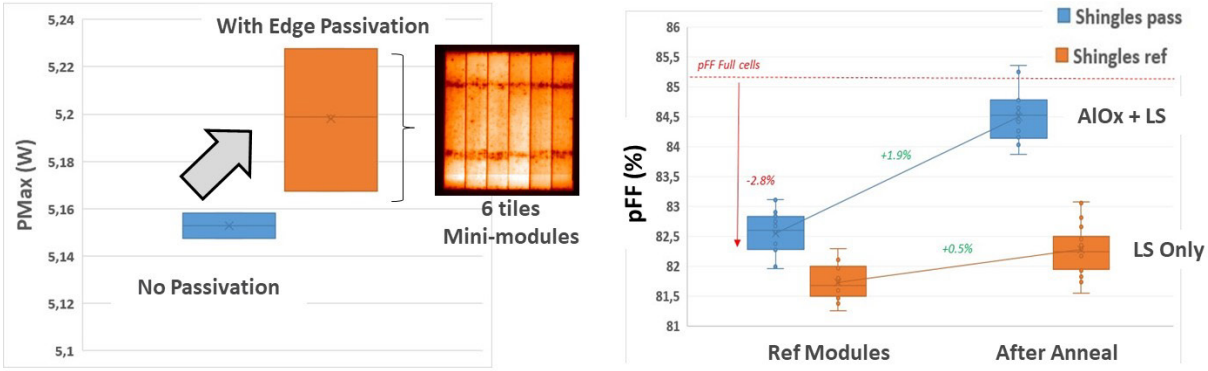


Figure 1. *Successful integration at module level of SHJ shingle cells integrating edge-passivation solutions (left). Performance boost seen at module level is directly linked to the presence of the passivation layer as shown by the pFF measurements conducted (right).*

It also demonstrates that despite the presence of the passivation layer over the metallization scheme, current can flow between the successive interconnected cells without significant increase of the series resistance. This is made possible by the fact that the AlO_X layer is not fully integer when deposited over the high aspect ratio metal lines, and this apparent local layer porosity allows the penetration of ECA through the AlO_X during interconnection and lamination, insuring electrical continuity in the string. However, as shown in Figure 2, if initial performances of “passivated” modules are promising, with such passivation configuration covering the metal pattern, strong impact on module overall reliability is clearly observed. A quick

and strong degradation of all modules is monitored already after 200 TC cycles. Exact mechanisms of module failure is not yet fully characterized, but the Fill Factor losses measured clearly indicates that the ohmic contact has been lost between the ECA and shingle metal grid. Adhesion of the ECA on the surface of the cell is also weakened by the presence of the AlO_X layer.

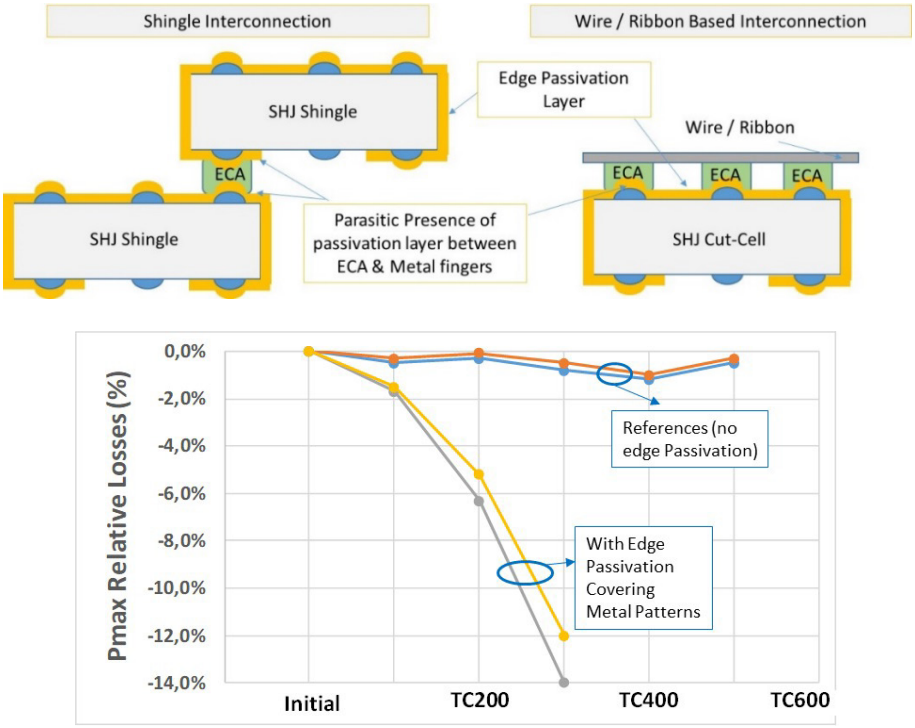


Figure 2. *Most Edge-passivation process explored in the literature, especially if ALD or PECVD deposition processes are used, generally lead to full/partial parasitic deposition of the layer over the cell metallization pattern (Top Schematics). Bottom Graph: Non-optimized edge passivation process can lead to strong degradation of final module reliability (TC ageing applied here on SHJ shingle modules).*

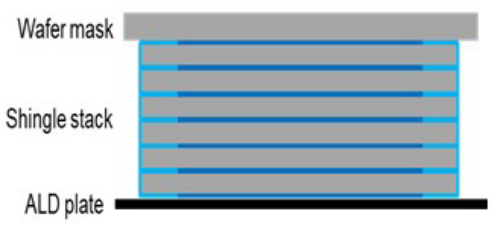
These results thus clearly show that specific care of edge-passivation deposition conditions has to be taken into account. In particular, it seems mandatory to avoid the deposition of the passivating layer in the interconnect area. As shown in next sections, several approaches can be considered to either localize the layer where it is needed (ie the cell cut-edge), or with more innovative approaches, insure the preservation of the interconnection by modifying the integration sequence of the AlO_X layer. Functional modules have been successfully manufactured for all three new edge passivation configurations studied and results obtained are described in more details in next sections.

4. How to localize the cut-edge passivation layer?

4.1 Edge passivation localization thanks to wafer stacking

To avoid the parasitic covering of metal during AlO_X deposition leading to reliability drop on final modules, we investigated the possibility to stack the shingle cells on our ALD equipment. Indeed, with such configuration, the cells are acting as shadowing masks for the surroundings wafers, limiting the flow of reactive gas species on the front and rear surfaces. Sacrificial cell or wafer is used for the top position. It is worth to note that this approach seems similar to recent industrial passivation tool proposed by SINGULUS [7] for which full process details are not yet disclosed. Due to the limited height of our ALD reactor, we were only able to test a full stack of 6-shingle cells (Figure 3). Each cut-cell is ~150µm thick, with usual SHJ shingle dimensions: 156mm length and 26mm width. This stack of wafer then undergoes the passivation

process described in previous section (15nm AlO_X + Light Soaking activation anneal), and associated final IV measurements extracted for each cell.



Cell parameters	V_{oc} (mV)	I_{sc} (A)	FF (%)	η (%)
Full cell	740.9	9.188	81.2	22.6
Cut cell	736.6	9.138	78.6	21.6
Edge passivated cell	742	9.151	81	22.5

Figure 3. *Left: schematic of the shingle cell stacking in the ALD reactor, the clear blue edges are covered with AlOx, the dark blue regions represents the uncovered surface of the cells. Right: IV measurements of the processed cell (initial, after-cut, after "stacked passivation").*

As shown in Figure 3, the efficiency recovery is excellent, and equivalent to previous published results available in the literature [8], [9]. The "stacked" passivated cell V_{OC} is even slightly better than the full cell. This could be explained by the cumulative beneficial effect of a light soaking process on SHJ cells [10] and the edge passivation process.

Hence, we clearly demonstrate that our low temperature shingle SHJ edge passivation protocol is still working properly with AlO_X localisation only on the edges. Nevertheless, despite several successive optimizations made on the wafer to wafer stacking placement, we can still observe a slight AlO_X parasitic overlap extending on both front and back surface of the cell's surfaces. If this is a clear improvement for standard ribbon/wire interconnection schemes where busbars are generally centered far from the edge, this remains problematic for shingle cells, where the bus bar to interconnect is located close to the edge. To avoid this specific issue for shingle, additional clamps are thus needed in the wafer stack, to offer extra-protection of the cell edge with regards to the parasitic deposition observed.

4.2 Optimized copper plating metallization

Again, objective is to avoid direct contact of ECA with the passivating layer. One interesting option would be the use of Copper electro-plating, especially the approach described in [11]. Indeed, with optimized process conditions, metal growth can be selectively done only over the initial metal lines, taking profit of local "cracks and defects" observed in the passivating layer when deposited over the printed seed-grid. This passivating layer is on the other hand highly resistive and perfectly integer on the rest of the wafer surface, and thus can avoid any parasitic ghost-plating that could occur over the ITO and more generally non-metallized cell surface.

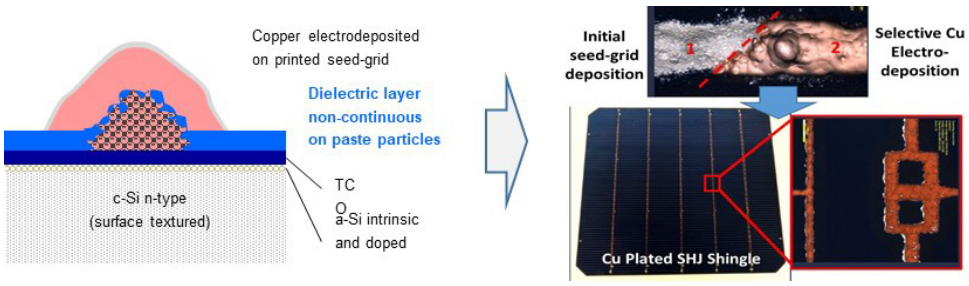


Figure 4. *With optimized Copper plating process, the growth of metal can occur through the top passivation layer, avoiding parasitic presence of such layer between the metal grid and the ECA used for interconnection.*

This approach thus cumulates several advantages: saving of silver consumption thanks to the copper plating, improved final cell/module performances thanks to the better conductivity of copper compared to silver coupled to the improved edge passivation, and finally, insure high final module reliability, as ECA is now in direct contact with the electrodeposited Copper metal.

4.3 Edge passivation after stringing?

Finally, if the main objective is to insure the proper conservation of the unique reliability properties of the shingle, why just simply not modify at all the interconnection integration scheme? We thus propose an alternative integration scheme, where the passivation layer would be deposited at the very end of the shingling process, directly on the finalized strings, and just before the encapsulation deposition and overall module lamination. This scheme has been tested on a few short strings (6-tile long shingle string) for a first proof of concept and to identify eventual process limitations: deposition uniformity issues, string potential breakage during deposition and subsequent layer annealing activation…etc.

Several mini-modules were successfully finalized with such passivated strings, and overall process feasibility proven with fully functional modules produced. Process optimization is still required though, as final output power remain slightly lower than best processed modules integrating individually passivated cells (Figure 6). Moreover, EL characterization conducted on the finalized strings show signs of local random edge degradation of the strings, probably not related to the passivation layer, but most probably to the excessive manual manipulation of strings needed to finalize this integration. Adapted automation should help to improve final module apparent defects, and probably improve overall reliability results obtained, as described in next section.

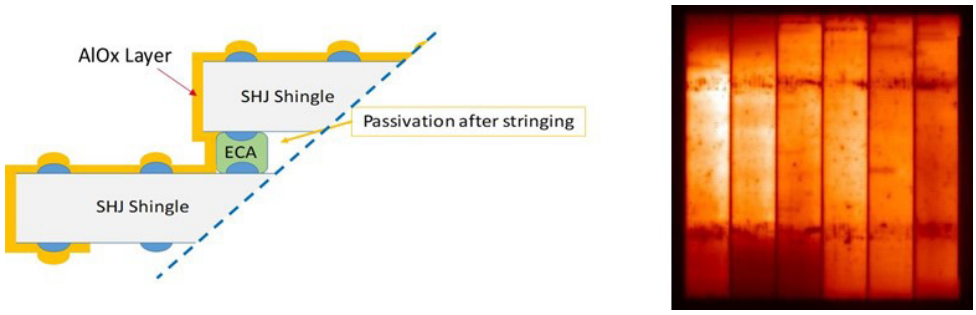


Figure 5. *Illustration of edge passivation process directly applied on interconnected strings. If functional modules have been manufactured in this configuration, EL characterization shows module local edge degradation probably linked to excessive manual manipulation of strings before lamination.*

5. Conclusions / Perspectives

As shown in previous sections, edge passivation is a promising solution to maximize the final performances of modules integrating cut-cells. This is even more true for SHJ shingle configuration, where small cell dimensions are needed, enhancing the sensitivity of the device to edge-related parasitic recombination. However, integration of such devices in final module is not straightforward. Indeed, if power boost is generally observed after module manufacturing thanks to the increased initial cell performances, we showed that if no proper localization of the layer is done (especially to avoid the deposition of the passivation layer in the interconnection area), strong degradation of reliability is observed on the monitored modules.

Three different localization approaches have been developed: stacking of the wafer during passivation layer deposition, passivation done directly over the interconnected string, and finally adaptation of specific plating process. In all three cases, functional modules have been manufactured, proving the integration feasibility of all explored concepts (Figure 6). If clear power improvement is measured for the “Stacked wafer” approach, impact of the passivation layer is much less obvious for the two other processes. In particular, as shown in section 3.3, EL images generated on “passivation on string” module concept reveal edge weaknesses, most probably related to the needed additional manual manipulation of the strings (that could be avoided with adapted automation). Partial delamination of ECA observed increases the

overall series resistances, and screen the passivation gain expected. Finally, for the third localization option, “metallization through passivation layer”, the plating process is not yet fully optimized, and the larger width of metal lines obtained on the tested cell after copper plating leads to increased shadowing (lower Isc). However, the increased module FF observed clearly demonstrates improved edge passivation performances, even if some of this FF gain can also be attributed to the reduced metal line resistance. Further overall process integration optimization would thus still be needed to fully benefit here from the edge-passivation boost expected in the last two localization options, but proof of concept already achieved already shows the feasibility and high potential of the three approaches explored.

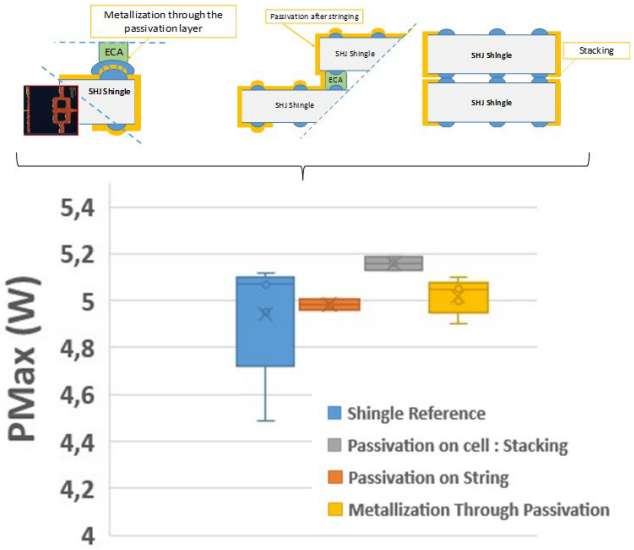


Figure 6. *Functional SHJ modules have been successfully manufactured for all three edge-passivation localization approaches explored.*

Moreover, as show in Figure 7, when edge passivation layer is properly localized, strong and immediate recovery of reliability is observed, with Thermal Cycling (TC) degradation perfectly comparable again with the reference modules. Indeed, up to 400 TC cycles have been applied so far on such modules, with again less than 2% performance losses observed. Only localization approach that still shows poor reliability behavior is the “passivation on string” concept, again probably linked to the cell to cell partial delamination observed because of the extra-manual manipulation of strings needed.

Finally, we thus demonstrated in this work, the possibility to properly combine excellent edge passivation up to module level with the reliability requirements needed to consider application of such processes to larger module volume and eventual further industrialization. Potential roadblocks and associated technological solutions have been described and discussed, showing the high potential of integrating edge-passivation solutions to the next generations of high-performance modules.

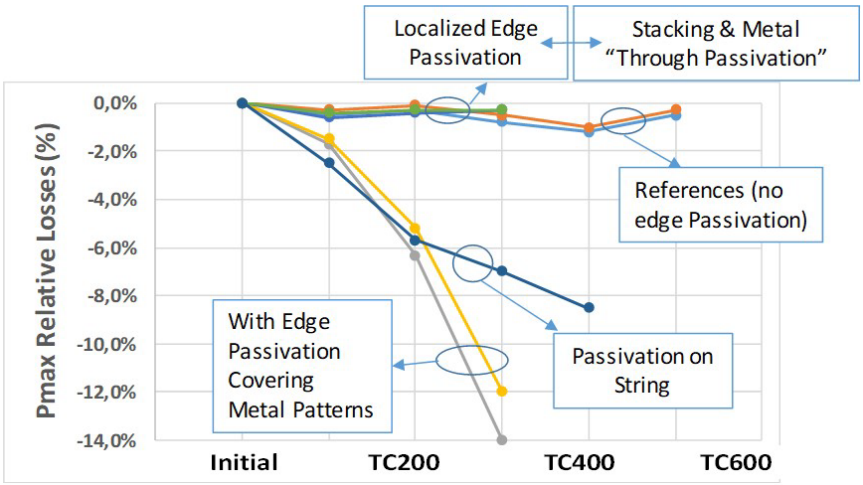


Figure 7. *Excellent reliability behavior can be fully recovered for modules integrating optimized localized-edge passivation solutions.*

Data availability statement

The data collected supporting the findings are available from the corresponding author upon reasonable request.

Author contributions

S. Harrison: project administration, conceptualization, methodology, formal analysis, investigation, writing – review & editing; **M. Albaric:** methodology, formal analysis, investigation, writing – review & editing; **V. Barth:** project administration, conceptualization, methodology, formal analysis, investigation, writing; **B. Martel:** conceptualization, methodology, formal analysis, investigation, writing; **M. Galiazzo:** conceptualization, methodology, resources; **N. Frasson:** conceptualization, methodology, resources; **A. Lachowicz:** conceptualization, methodology, resources.

Competing interests

Authors declare no competing interests in the writing of this proceeding paper.

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